WHAT IS CLAIMED IS:

1. A multi-processing system comprising:

n processors, each said processor operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to or from one or more addressable memories;

m memory sources, each memory source having a unique addressable space;

a switch matrix having links connected to said memories and connected to said processors; and

wherein each processor has at least two data ports and wherein one of said data ports is connected through said switch matrix to all of said data memories and wherein the other of said data ports is connected to a specific subset of said data memories.

2. The processing system set forth in Claim 1 wherein said connection to each said data memory subset is via one or said split links of said switch matrix.

3. The processing system set forth in Claim 1 wherein each sad processor includes at least one instruction port.

4. The processing system set forth in Claim 1 wherein said instruction port of each said processor is connectable via a specific dedicated link of said switch matrix to a specific instruction memory.

5. The processor set forth in Claim 4 wherein said switch matrix is further operable for inhibiting a connection from each said dedicated instruction link to said specific memory and instead enabling a common connection from said instruction port of all said processors to a common instruction memory.

6. The system set forth in Claim 1 wherein said switch matrix includes crosspoints for interconnecting said links and wherein said n processors, said m memory sources and said switch matrix, including said links and said crosspoints are all constructed on a single chip, and wherein said links and said crosspoints of said switch matrix are distributed across said chip in spatial relationship with said n processors and said m memories.

7. A multi-processing system comprising:

n processors, each said processor operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to or from one or more addressable memories;

m memory sources, each memory source having a unique addressable space;

a switch matrix having links connected to said memories and connected to said processors; and

circuitry, including splitting at least one of said links of said switch matrix, for selectively and concurrently interconnecting any of said processors with any of said memories for the interchange between said memories and said connected processors of instruction streams from one or more memory addressable spaces and data from other addressable memory spaces.

8. The processing system set forth in Claim 7 where m is greater than n.

9. The processor set forth in Claim 7 wherein said switch matrix contains a plurality of crosspoints operable on a cycle by cycle basis to effect said interconnecting of processors and memories.

10. The processor set forth in Claim 9 wherein said switch matrix further includes circuitry for responding to provided addresses for controlling said crosspoints.

11. The processor set forth in Claim 7 wherein each processor has at least two data ports and at least one instruction port, and wherein one of said data ports is connected through said switch matrix to all of said data memories and wherein the other of said data ports is connected to a specific subset of said data memories.

12. The processor set forth in Claim 11 wherein said connection to each said data memory subset is via one of said split links of said switch matrix.

13. The processor set forth in Claim 11 wherein said instruction port of each said processor is connectable via a specific dedicated link of said switch matrix to a specific instruction memory.

14. The processor set forth in Claim 13 wherein said switch matrix is further operable for inhibiting a connection from each said dedicated instruction link to said specific memory and instead enabling a common connection from said instruction port of all said processors to a common instruction memory.

15. The processor set forth in Claim 7 wherein said split links can be connected together on a cycle by cycle basis.

16. The processor set forth in Claim 9 wherein each said crosspoint includes prioritization control circuitry to sequence simultaneous processor access attempts to the same memory.

17. The processor set forth in Claim 16 wherein said prioritization circuitry includes sequential token passing.

18. The processor set forth in Claim 17 wherein said token passing includes circuitry for insuring lowest priority memory access to the processor which last successfully assessed the memory assembled with said crosspoint.

19. The processor set forth in Claim 18 further comprising circuitry, including said token passing circuitry, for allowing a separate processor to have access to any of said instruction or data memories over said switch matrix links.

20. The processor set forth in Claim 18 further comprising circuitry for allowing a separate processor to have access to any of said instruction or data memories over said switch matrix links and wherein said prioritization circuitry further includes circuitry for giving lowest priority to said separate processor for each said memory.

21. The system set forth in Claim 7 wherein said switch matrix includes crosspoints for interconnecting said links and wherein said n processors, said m memory sources and said switch matrix, including said links and said crosspoints, are all constructed on a single chip, and wherein said links and said crosspoints of said switch matrix are distributed across said chip in spacial relationship with said n processors and said m memories.

22. A method of operating a multi-processing system having n processors, each said processor operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to or from one or more addressable memories;

m memory sources, each memory source having a unique addressable space;

a switch matrix having links connected to said memories and connected to said processors, each said processor having at least two data ports, said method comprising the steps of:

splitting at least one of said links of said switch matrix; and

connecting one or said data ports through said switch matrix to all of said data memories; and

connecting the other of said data ports through said split links of said switch matrix to a specific subset of said data memories.

23. The method set forth in Claim 22 wherein said switch matrix contains a plurality of crosspoints and wherein said method includes the step of:

operating said crosspoints on a cycle-by-cycle basis to effect said interconnecting of processors and memories.

24. The method set forth in Claim 23 further including the step of:

responding to provided addresses for controlling said crosspoints.

25. The method set forth in Claim 24 wherein each said processor has at least one instruction port and wherein said method further includes the step of:

connecting said instruction port of each said processor via a specific dedicated link of said switch matrix to a specific instruction memory.

26. The method set forth in Claim 25 further including the steps of:

inhibiting a connection from each said dedicated instruction link to said specific memory; and

concurrently enabling a common connection from said instruction port of all said processors to a common instruction memory.

27. The method set forth in Claim 22 further including the step of:

connecting together said split links on a cycle-by-cycle basis.

28. The method set forth in Claim 22 wherein each said crosspoint includes a prioritization control system and wherein said method further includes the step of:

sequencing simultaneous processor access attempts to the same memory.

29. The method set forth in Claim 28 wherein said prioritization system includes the step of sequential token passing.

30. The method set forth in Claim 29 wherein said token passing step includes the step of:

insuring lowest priority memory accessed to the processor which last successfully assessed the memory associated with said crosspoint.

31. A method of operating a multi-processing system having n processors, each said processor operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to or from one or more addressable memories;

m memory sources, each memory source having a unique addressable space;

a switch matrix having links connected to said memories and connected to said processors, said method comprising the steps of:

splitting at least one of said links of said switch matrix; and

selectively and concurrently interconnecting any of said processors with any of said memories, and interchanging over said selective interconnections instruction streams from one or more of said addressable memory spaces and data from other of said addressable memory spaces.

32. The method set forth in Claim 31 wherein said switch matrix contains a plurality of crosspoints and wherein said method includes the step of:

operating said crosspoints on a cycle by cycle basis to effect said interconnecting of processors and memories.

33. The method set forth in Claim 32 further including the step of:

responding to provided addresses for controlling said crosspoints.

34. The method set forth in Claim 31 wherein each processor has at least two data ports and at least one instruction port, and wherein said method further includes the steps of:

connecting one of said data ports through said switch matrix to all of said data memories; and

connecting the other of said data ports through said split links of said switch matrix to a specific subset of said data memories.

35. The method set forth in Claim 34 further including the step of:

connecting said instruction port of each said processor via a specific dedicated link of said switch matrix to a specific instruction memory.

36. The method set forth in Claim 35 further including the steps of:

inhibiting a connection from each said dedicated instruction link to said specific memory; and

concurrently enabling a common connection from said instruction port of all said processors to a common instruction memory.

37. The method set forth in Claim 35 further including the step of:

connecting together said split links on a cycle-by-cycle basis.

38. The method set forth in Claim 32 wherein each said crosspoint includes a prioritization control system and wherein said method further includes the step of:

sequencing simultaneous processor access attempts to the same memory.

39. The method set forth in Claim 38 wherein said prioritization system includes the step of sequential token passing.

40. The method set forth in Claim 39 wherein said token passing step includes the step of:

insuring lowest priority memory accessed to the processor which last successfully accessed the memory associated with said crosspoint.

41. The method set forth in Claim 40 further comprising the step of:

allowing separate processors to have access to any of said instruction or data memories over said switch matrix links, and wherein said prioritization system further includes the step of giving lowest priority to said separate processor for each said memory.

42. An image processing system, including a master processor for controlling said system, said system including a multi-processing system comprising:

n processors, each said processor operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to or from one or more addressable memories;

m memory sources, each memory source having a unique addressable space;

a switch matrix having links connected to said memories and connected to said processors; and

circuitry, including splitting at least one of said links of said switch matrix, for selectively and concurrently interconnecting any of said processors with any of said memories for the interchange between said memories and said connected processors of instruction streams from one or more addressable memory spaces and data from other addressable memory spaces.

43. The system set forth in Claim 42 further including an external memory and wherein said master processor and said parallel processors communicate to said external memory via a transfer processor and all processors can communicate to each other via said switch matrix via said internal memory spaces.